

**Figure 1**

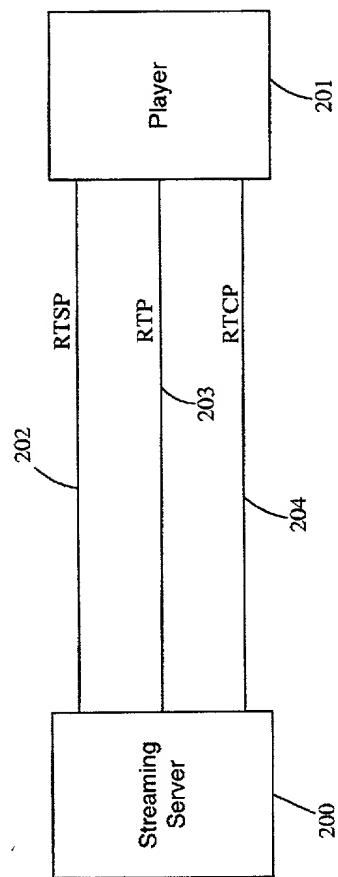
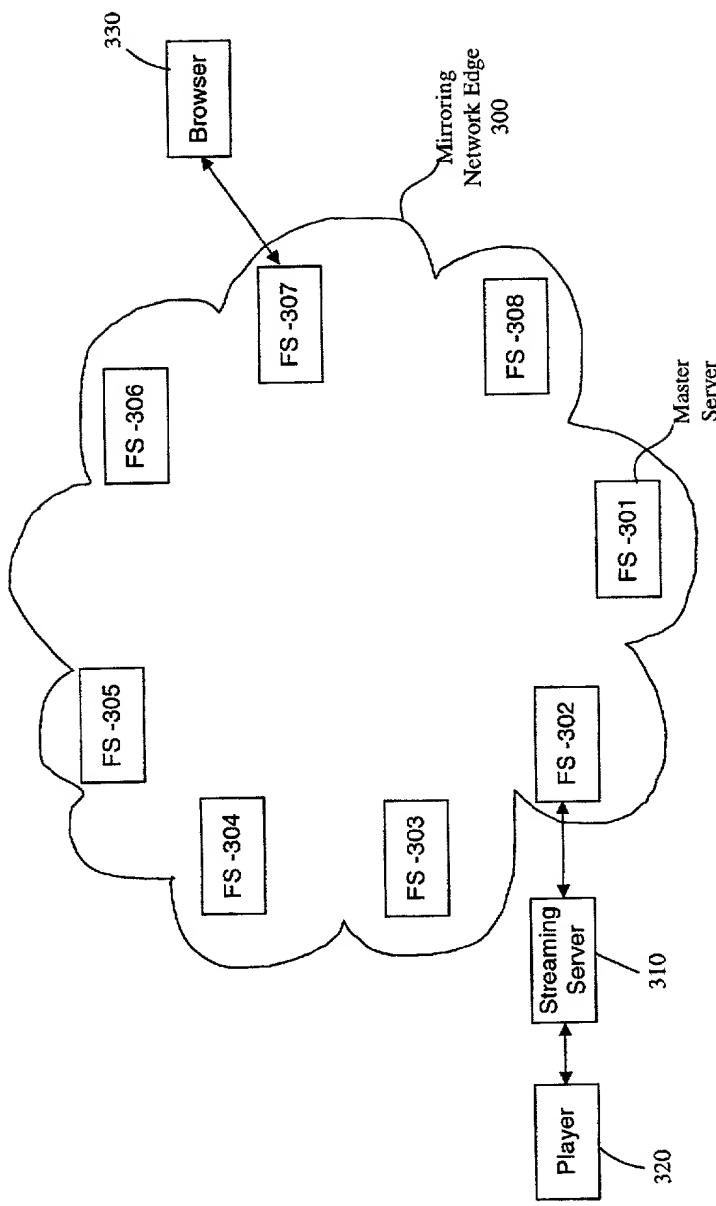


Figure 2



**Figure 3**

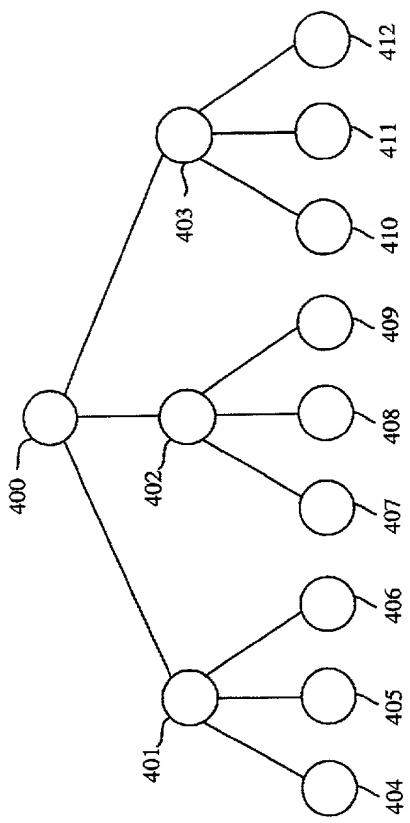
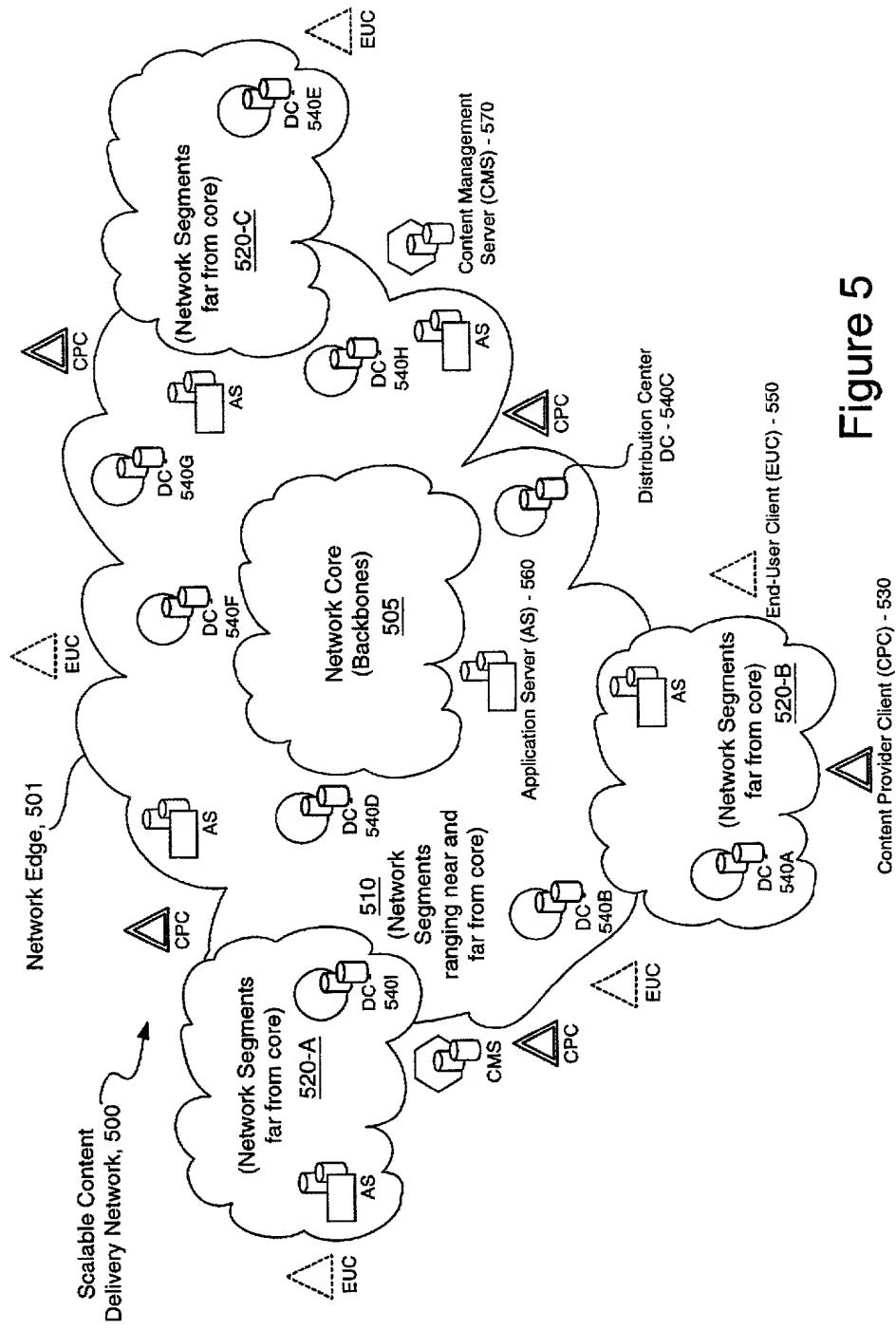
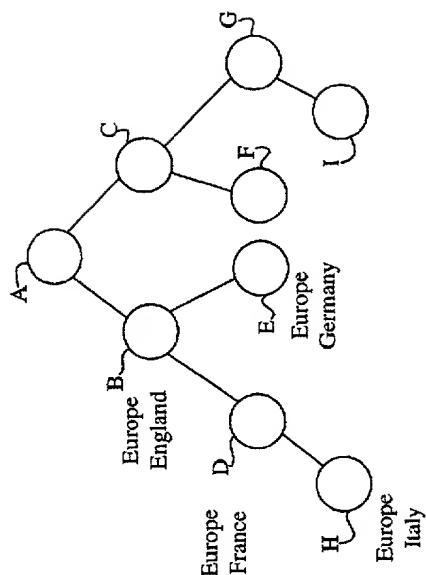


Figure 4



**Figure 5**



**Figure 6**

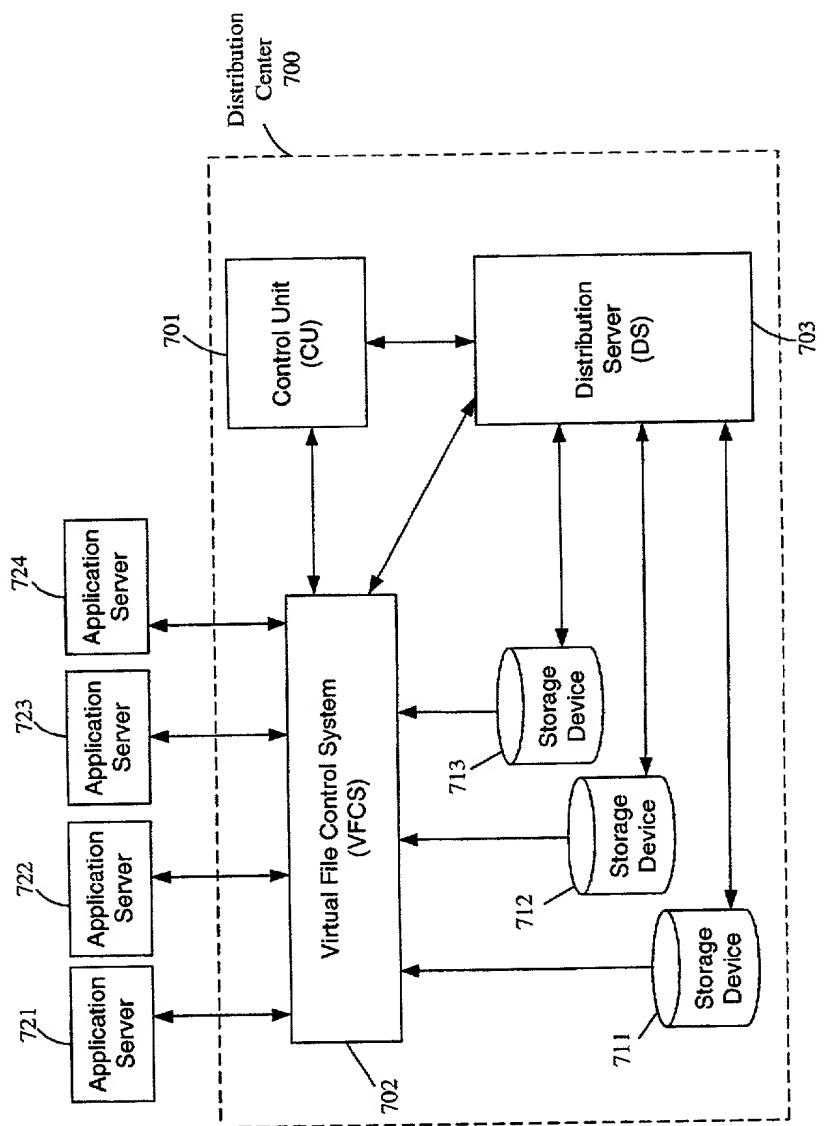


Figure 7

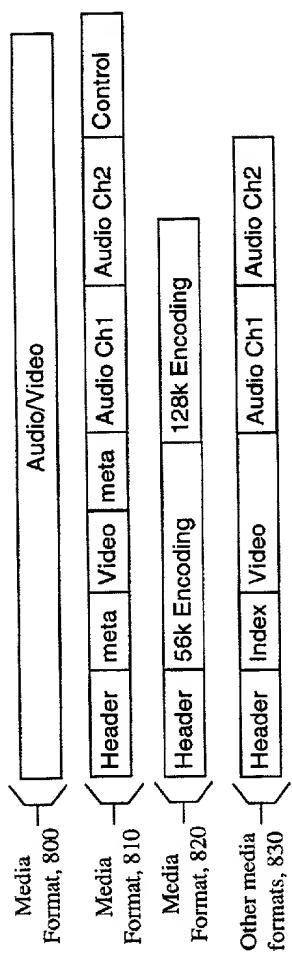


Figure 8

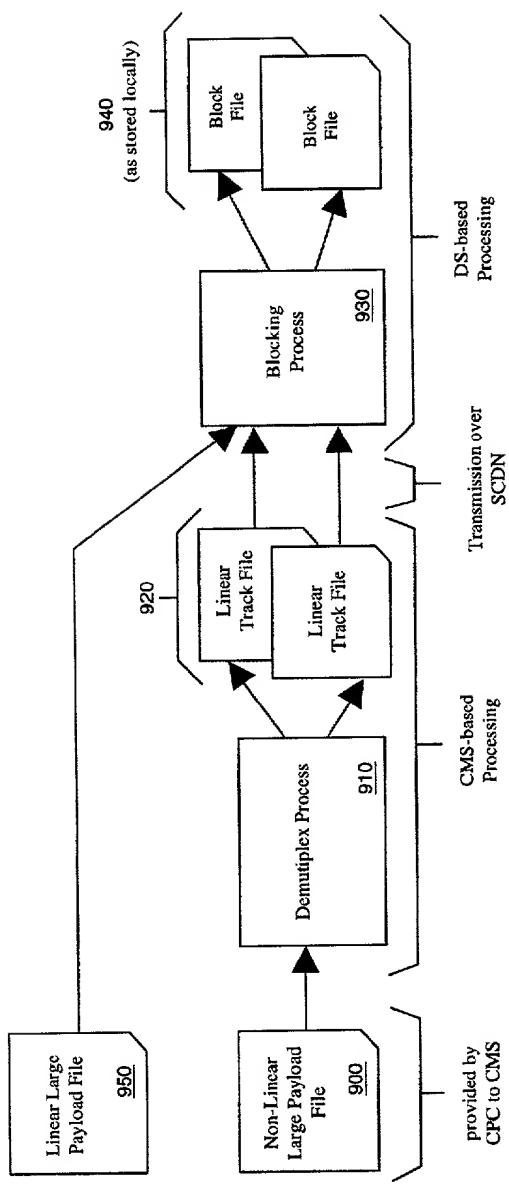


Figure 9

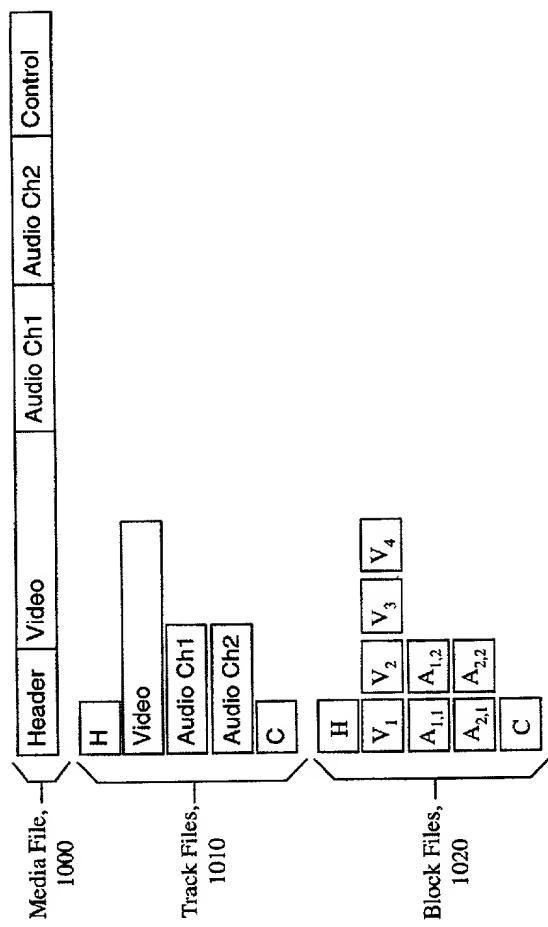


Figure 10

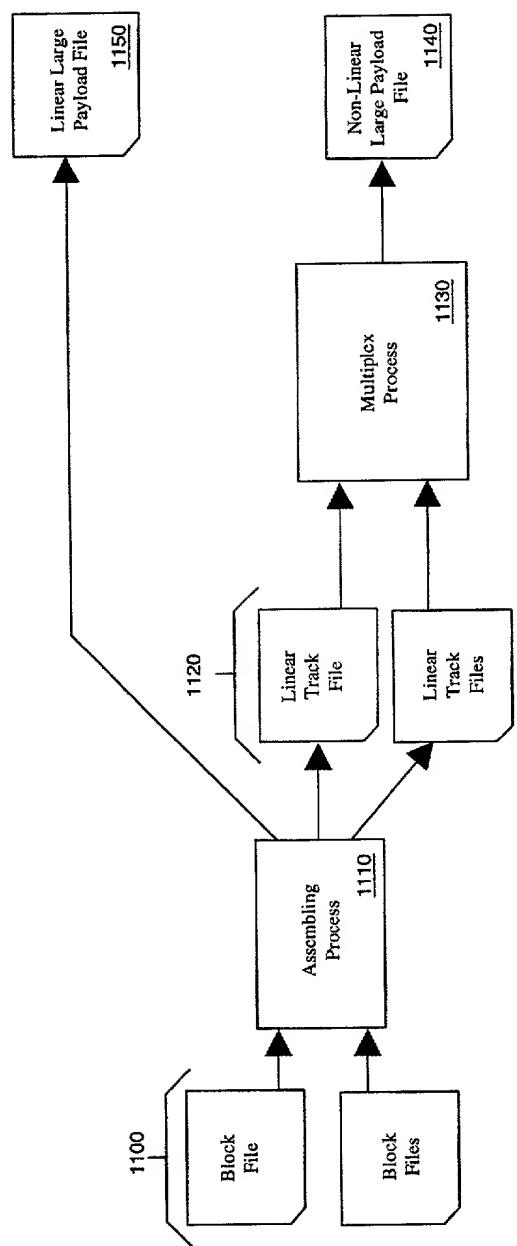


Figure 11

Bit Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Attribute B	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Attribute D	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0
Attribute E	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0
Attribute H	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1
Rolled Up Attribute D	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1
Rolled Up Attribute B	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1

**Figure 12**

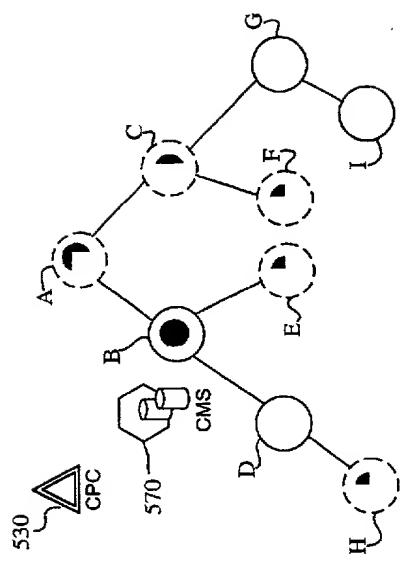
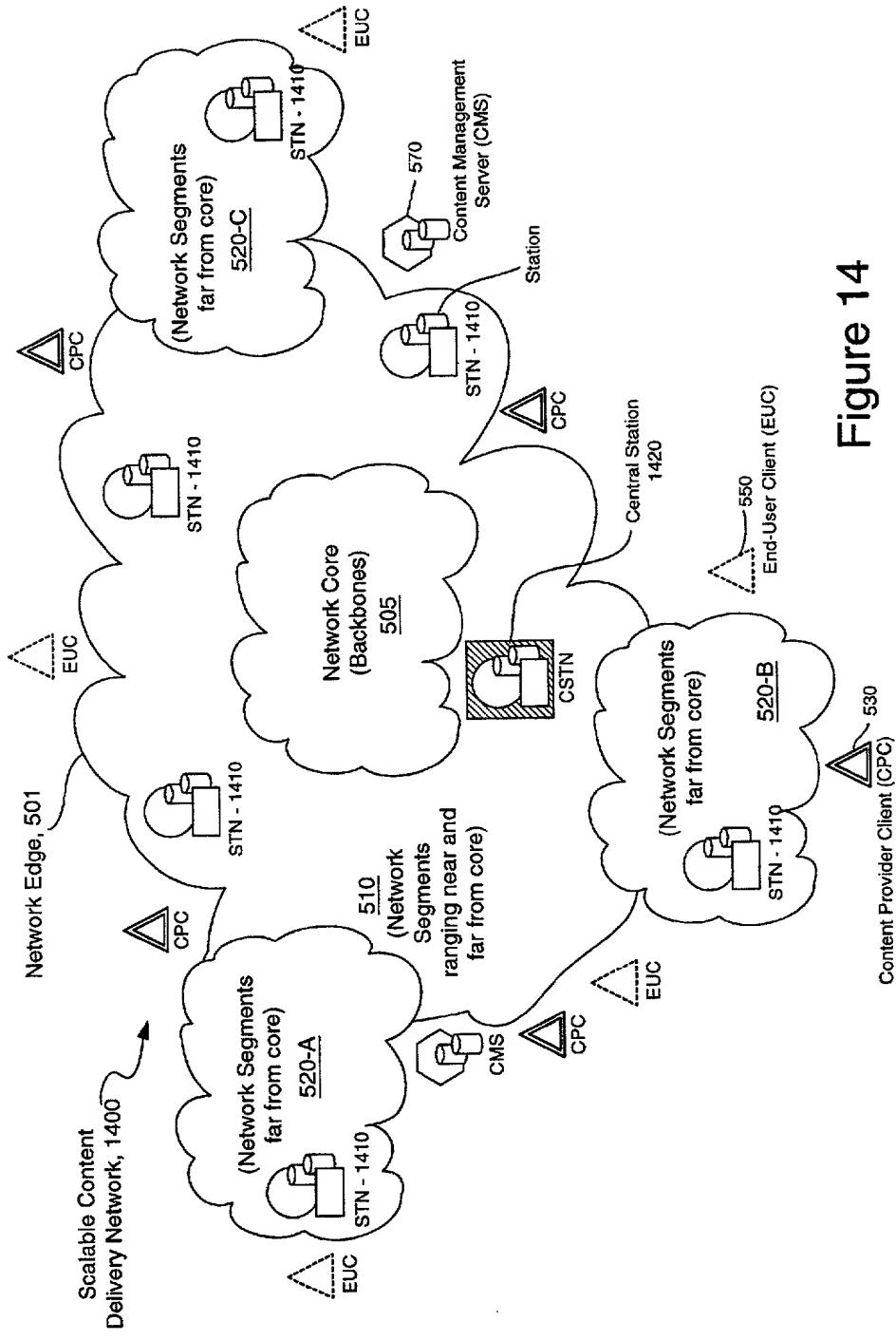


Figure 13



**Figure 14**

Figure 15

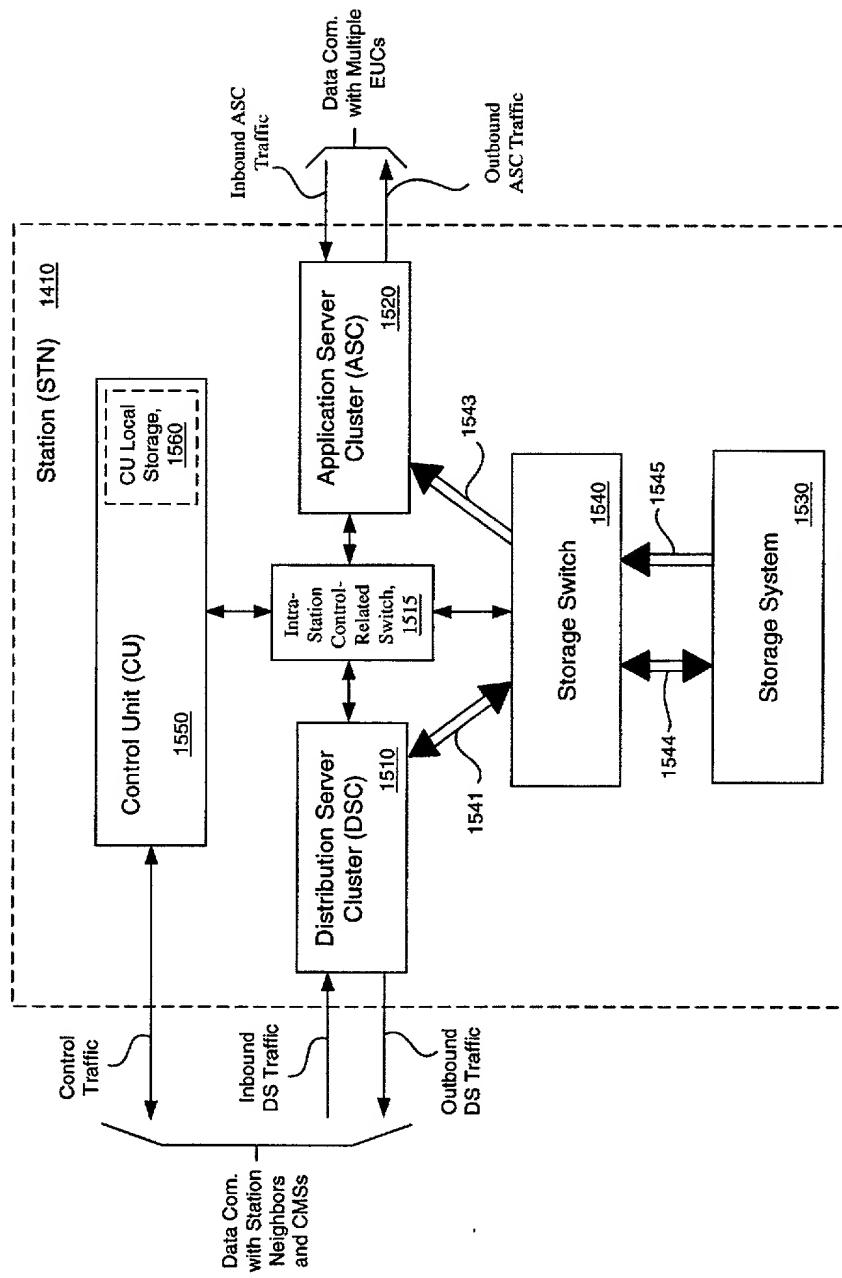
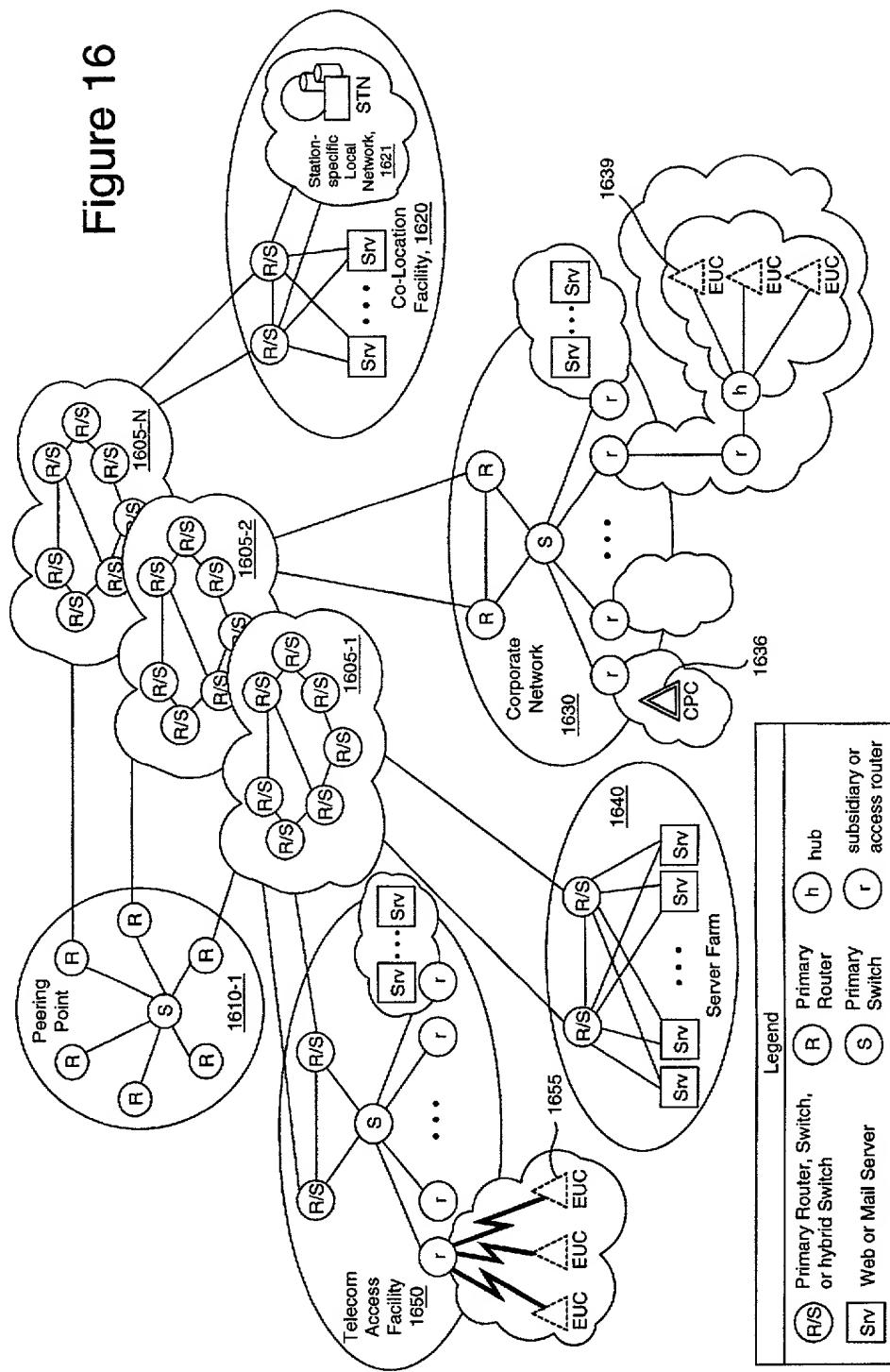


Figure 16



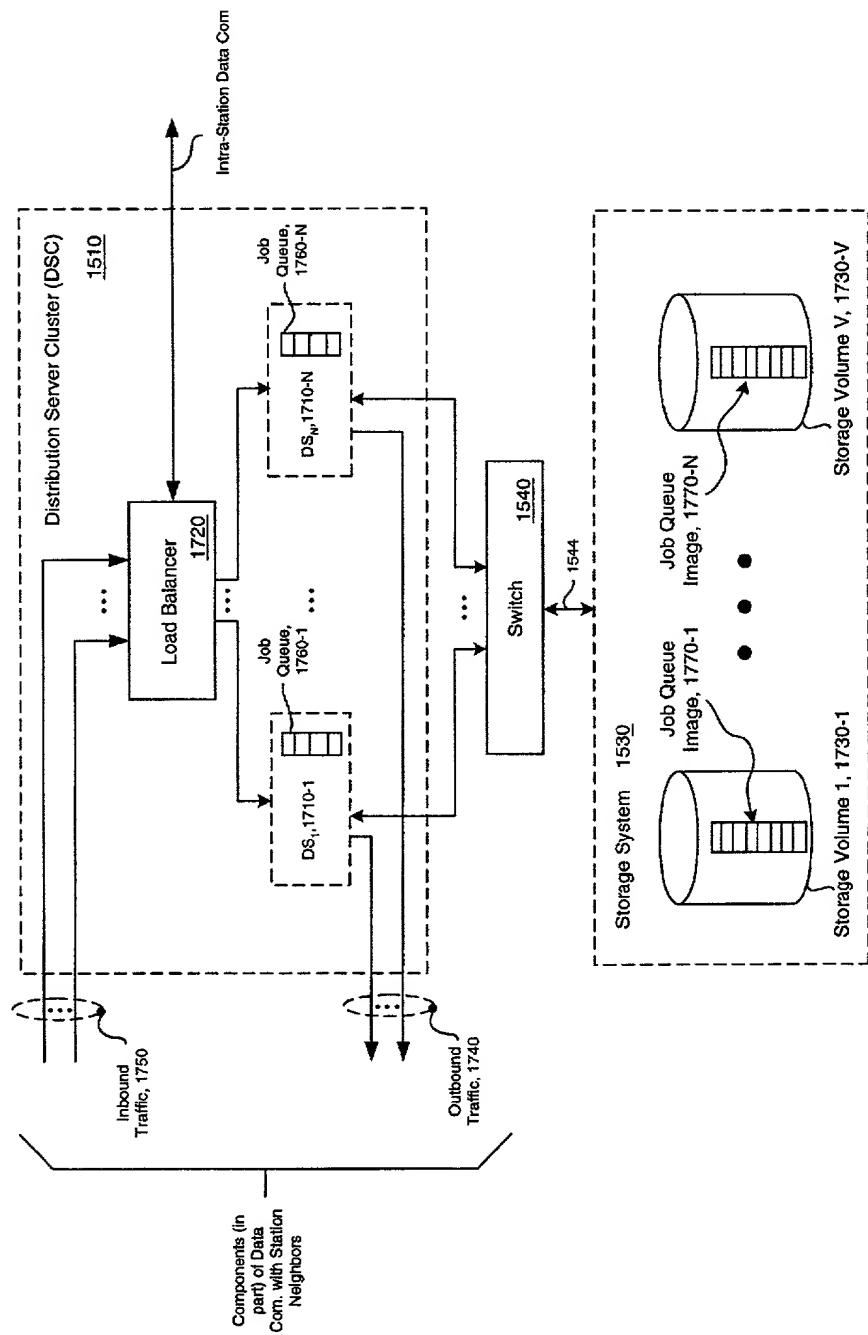
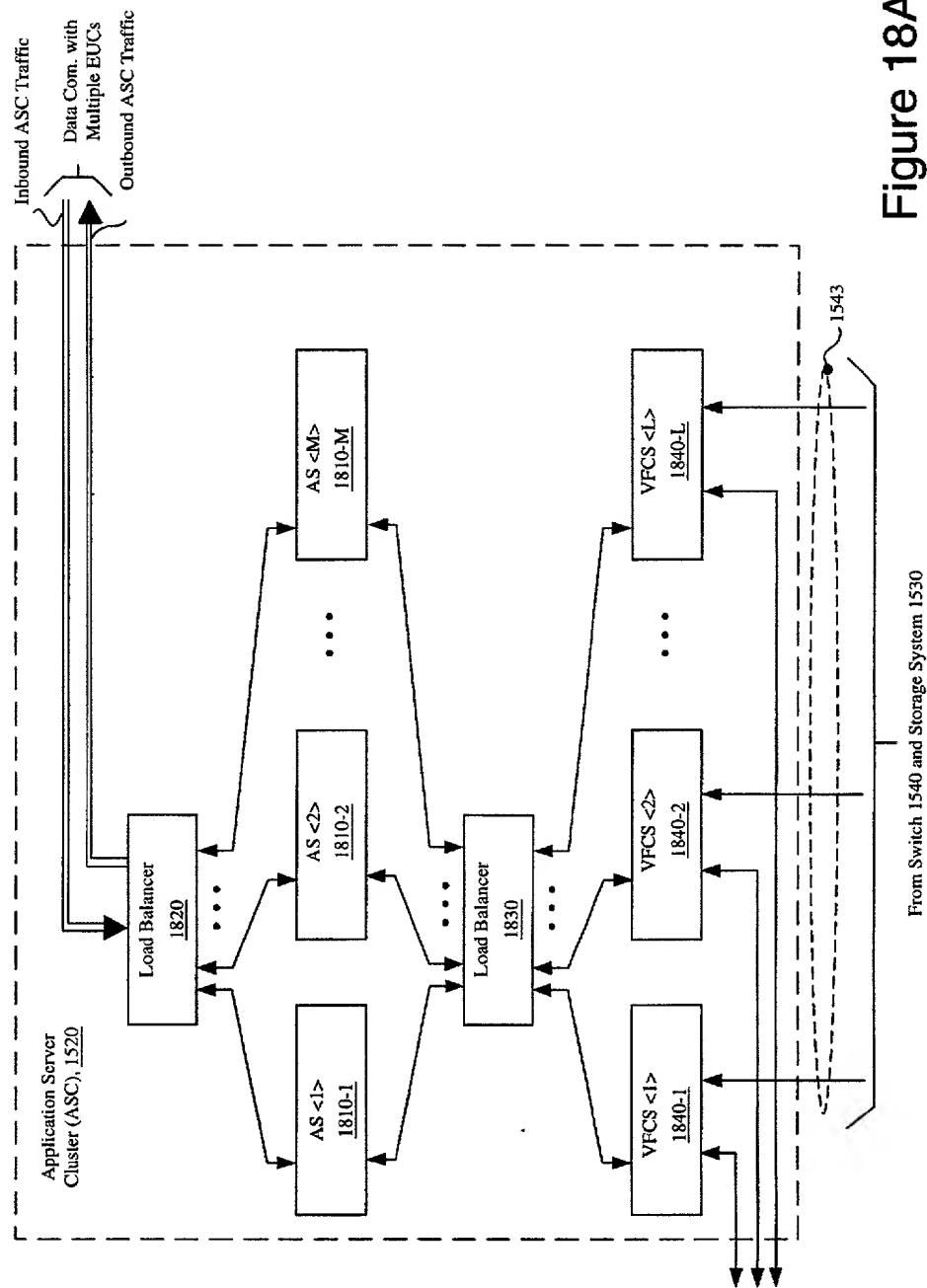


Figure 17

Figure 18A



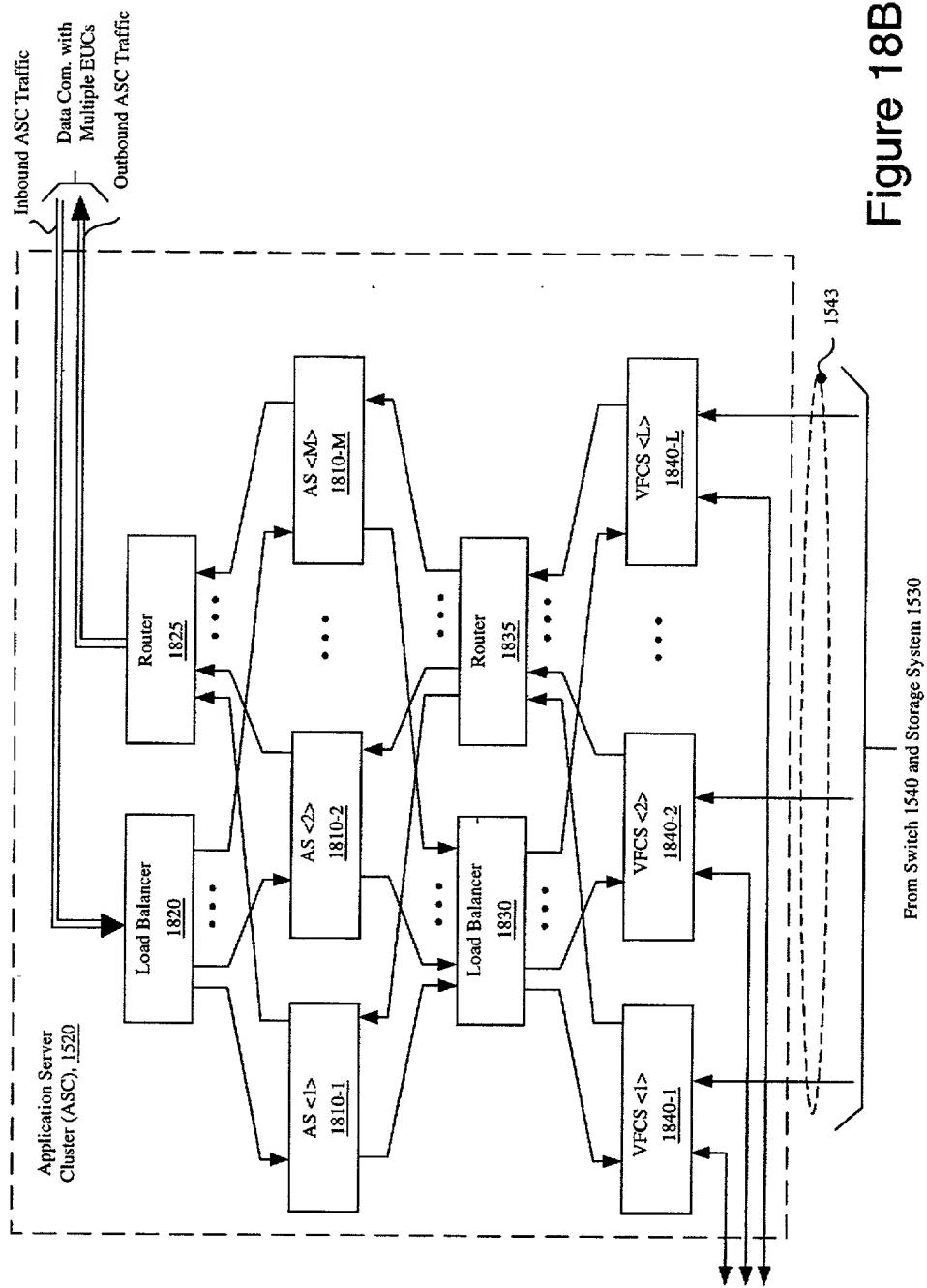


Figure 18B

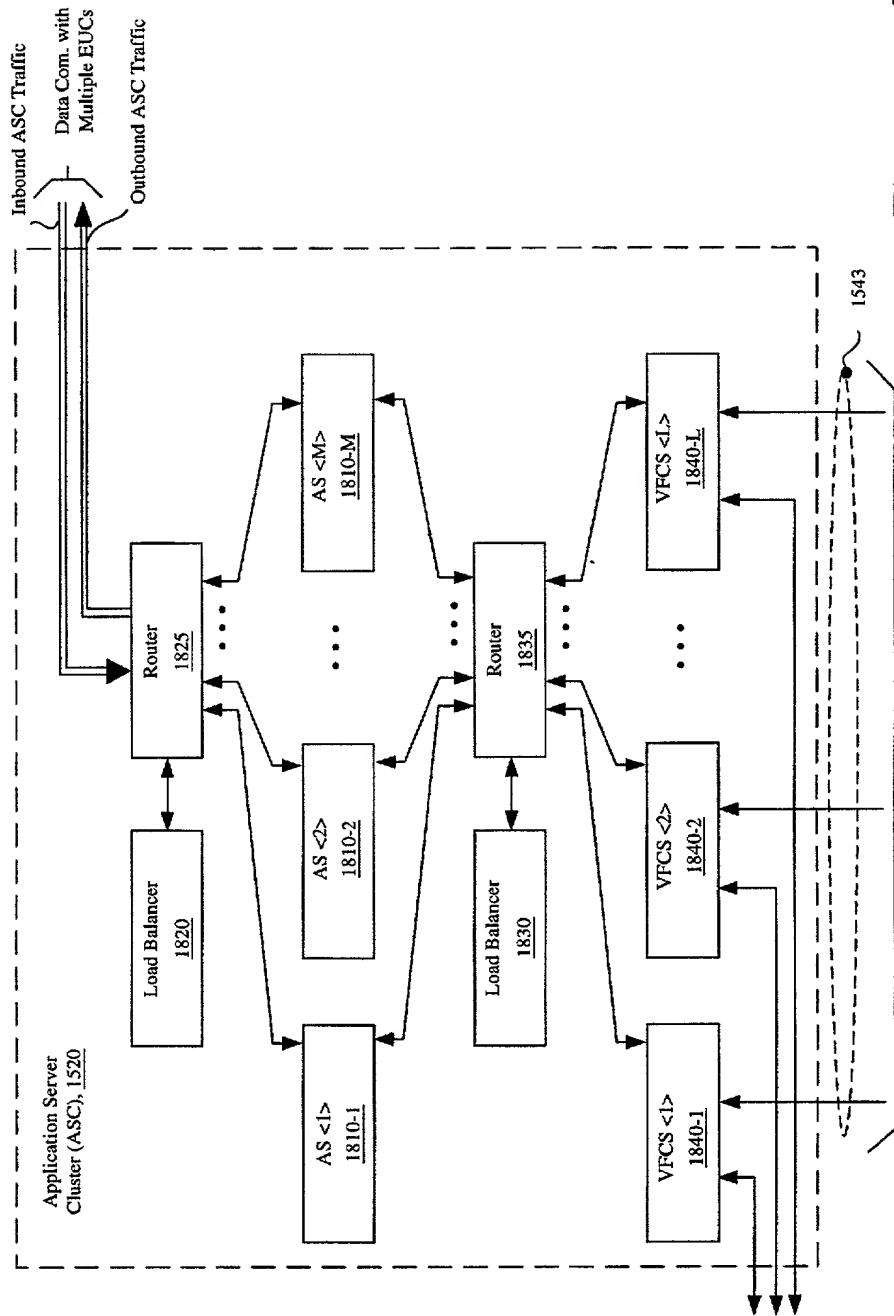


Figure 18C

From Switch 1540 and Storage System 1530

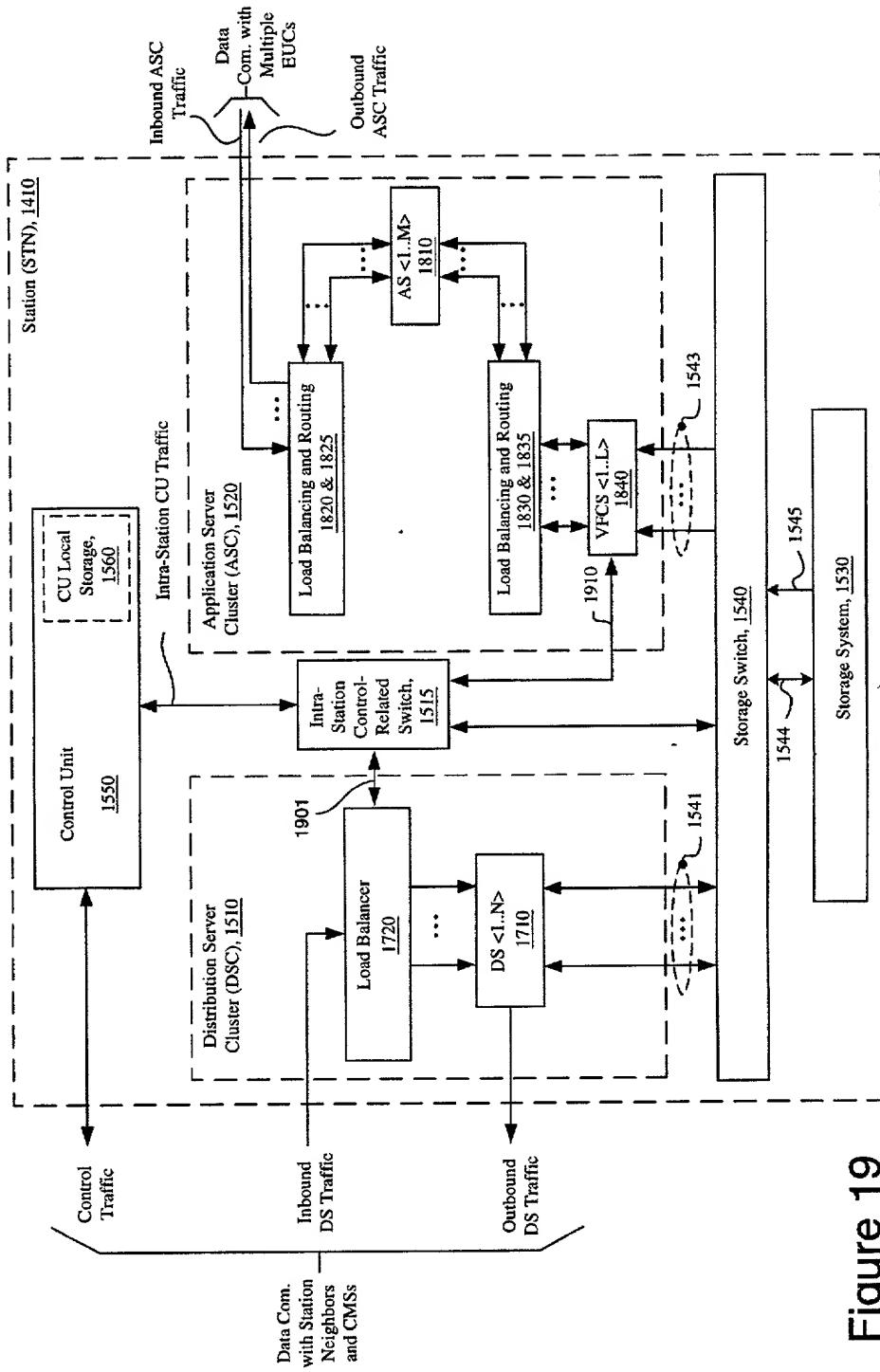


Figure 19

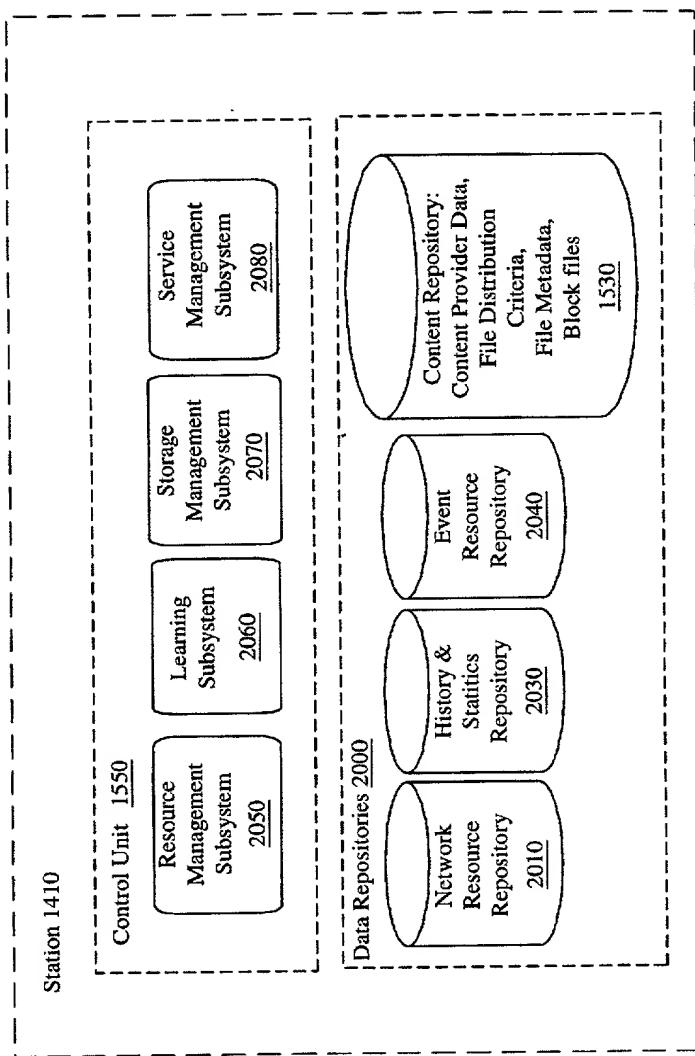


Figure 20

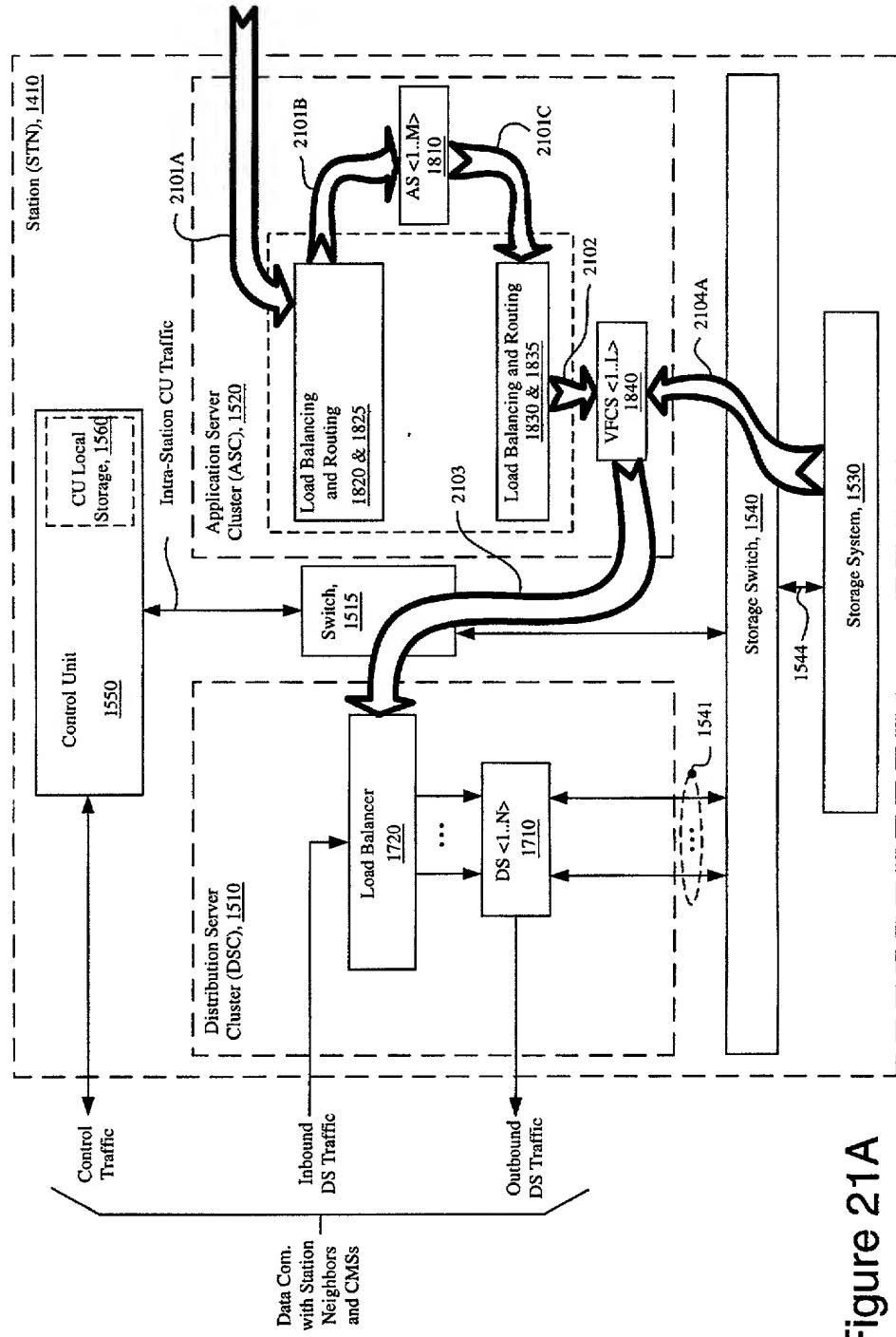


Figure 21A

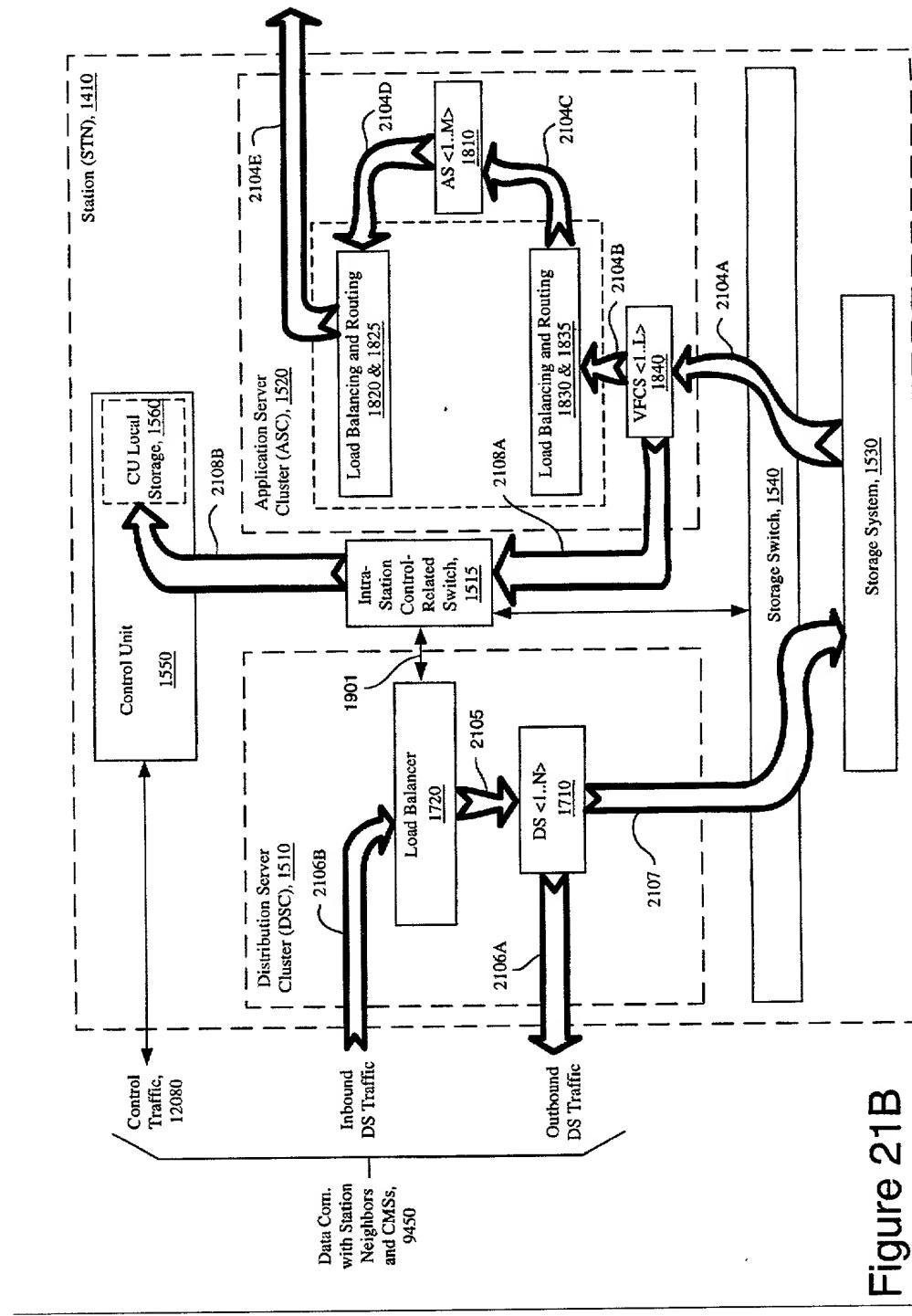


Figure 21B

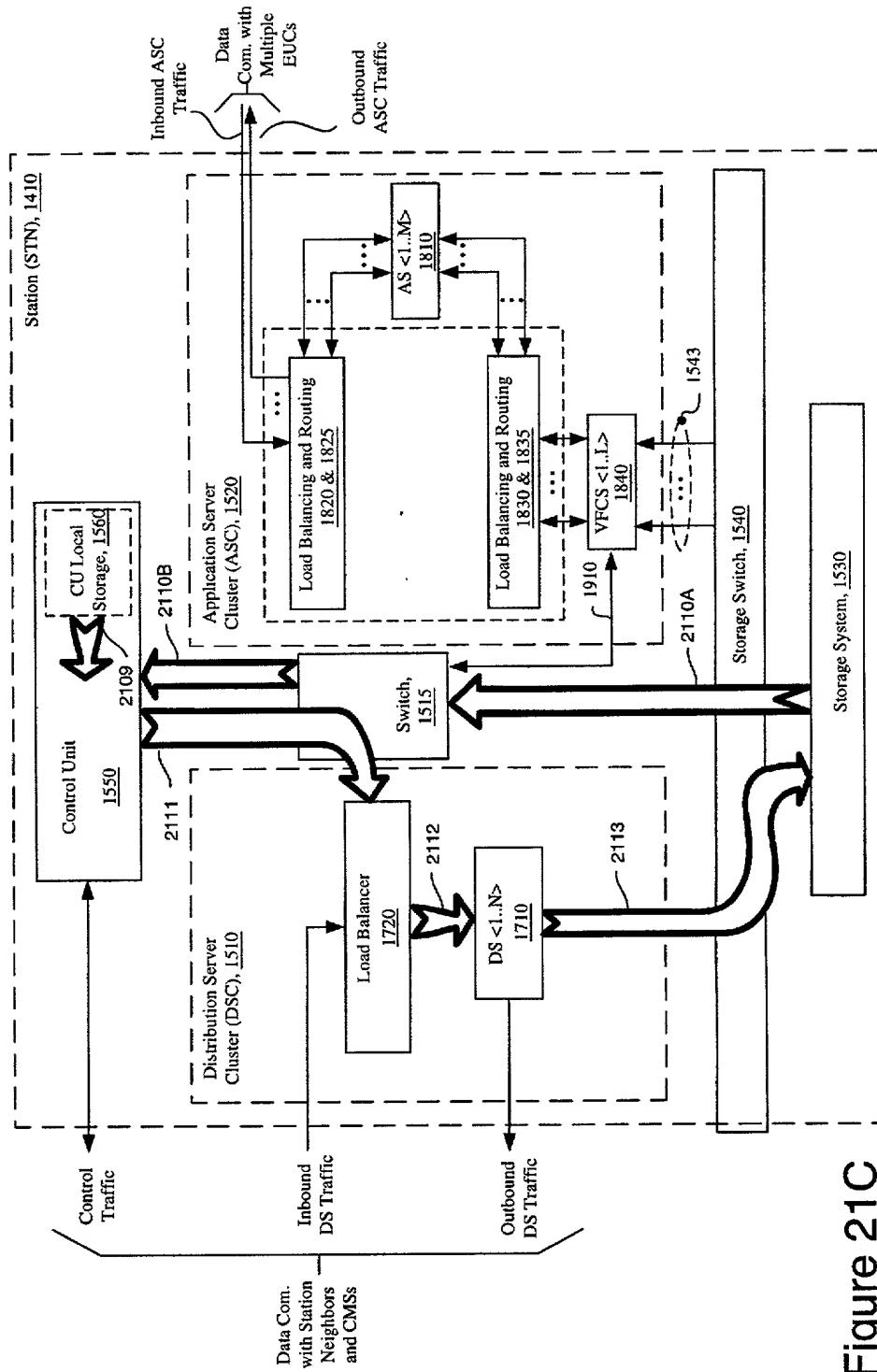


Figure 21C

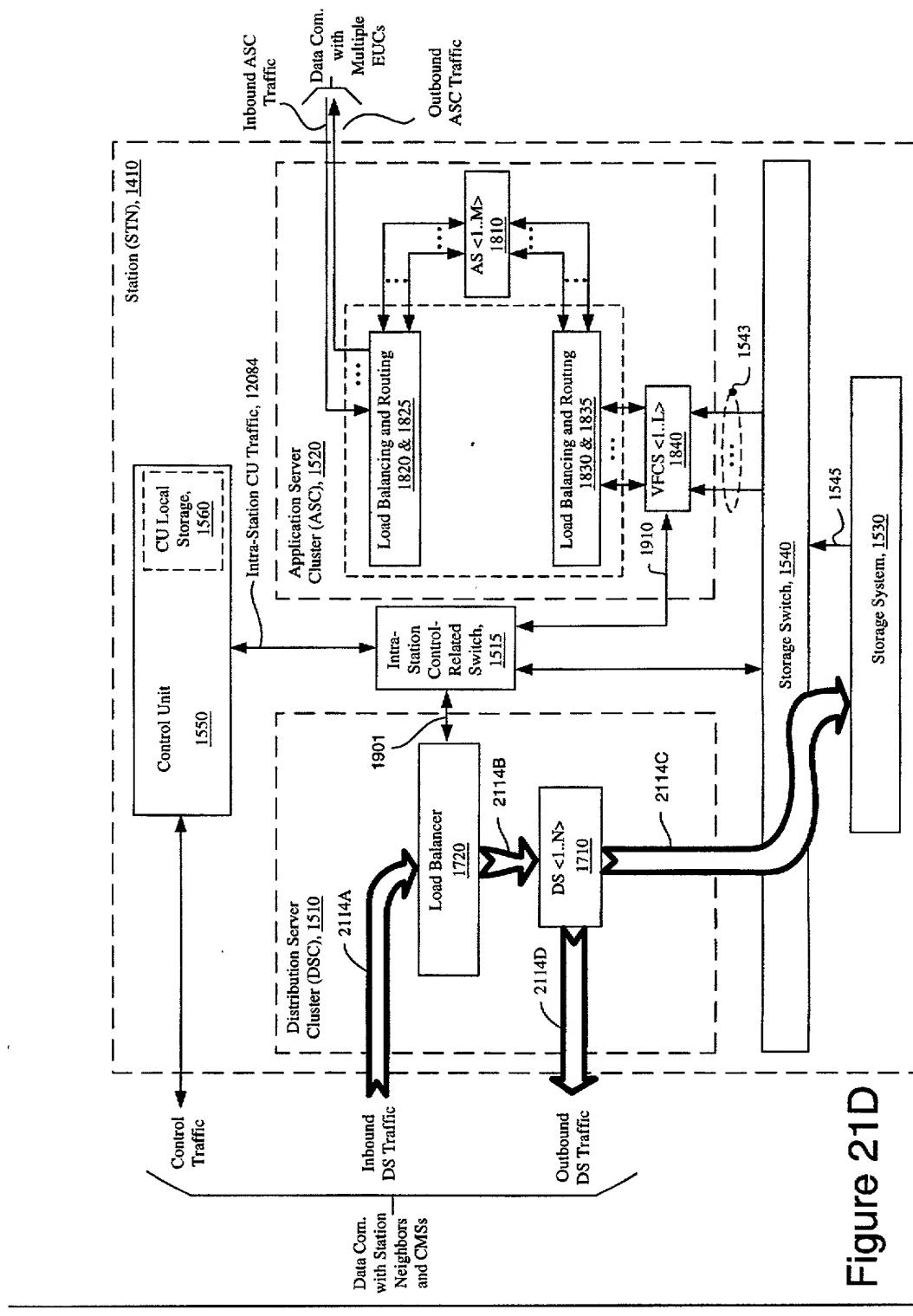
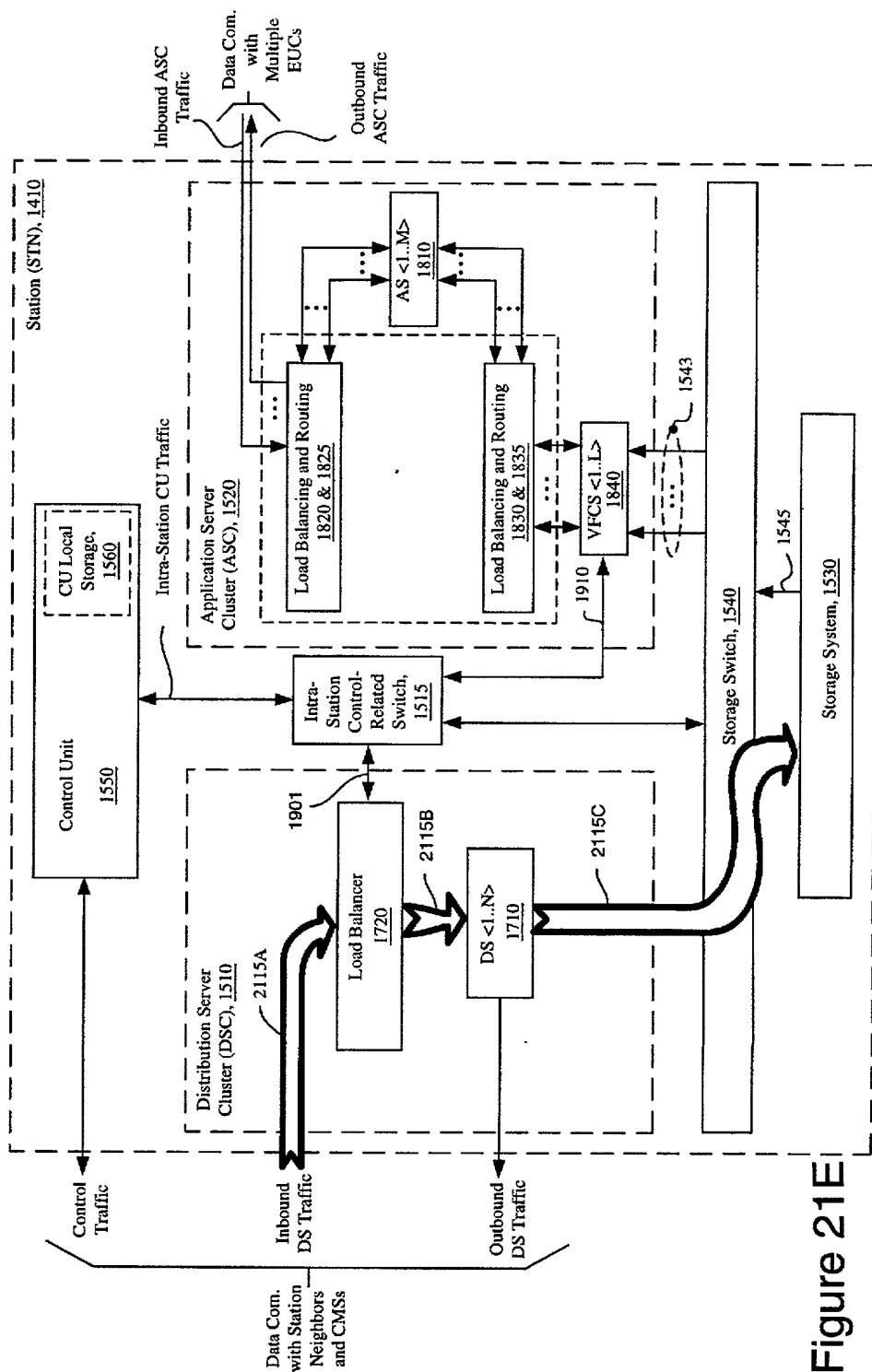


Figure 21D



**Figure 21E**

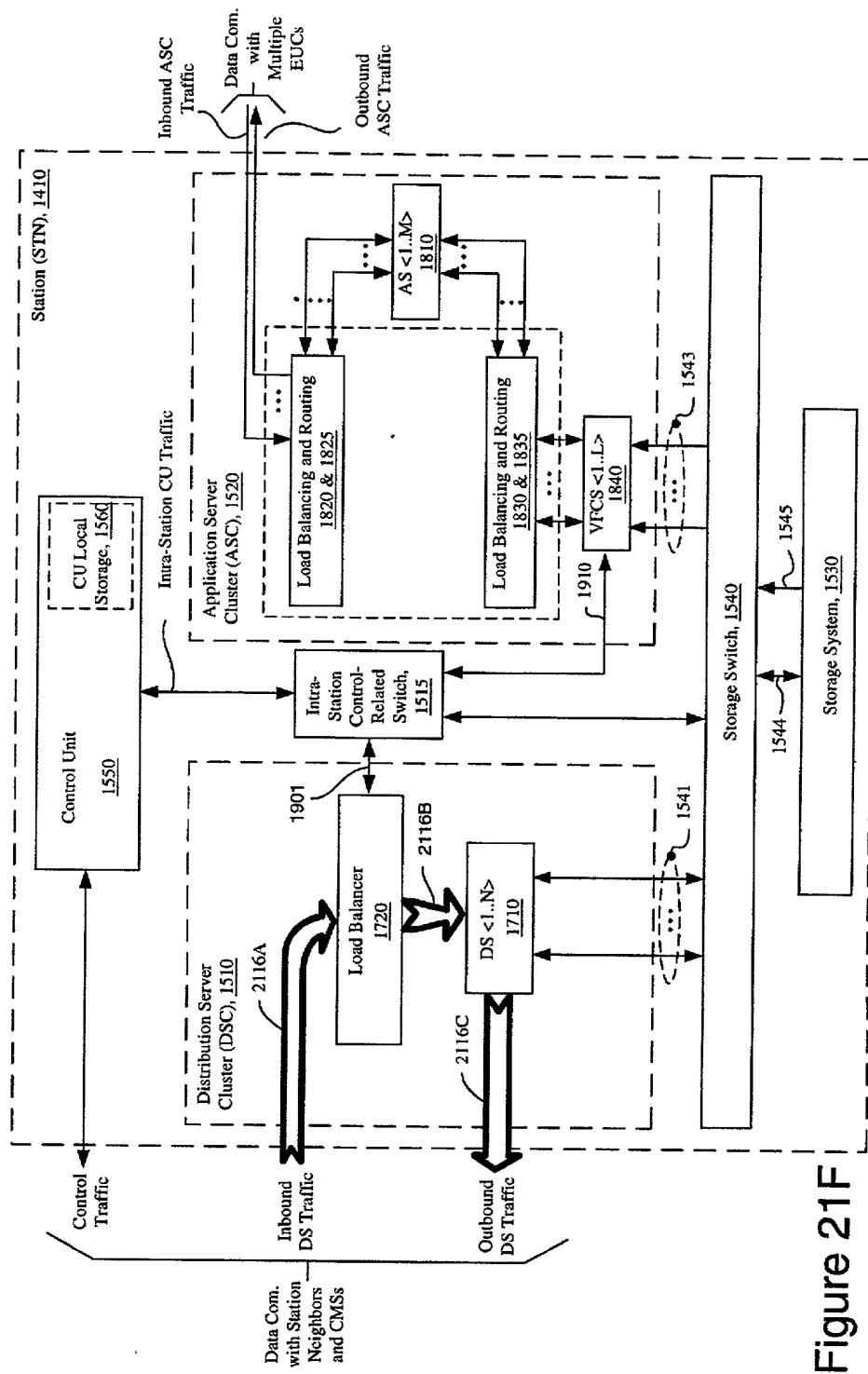


Figure 21F

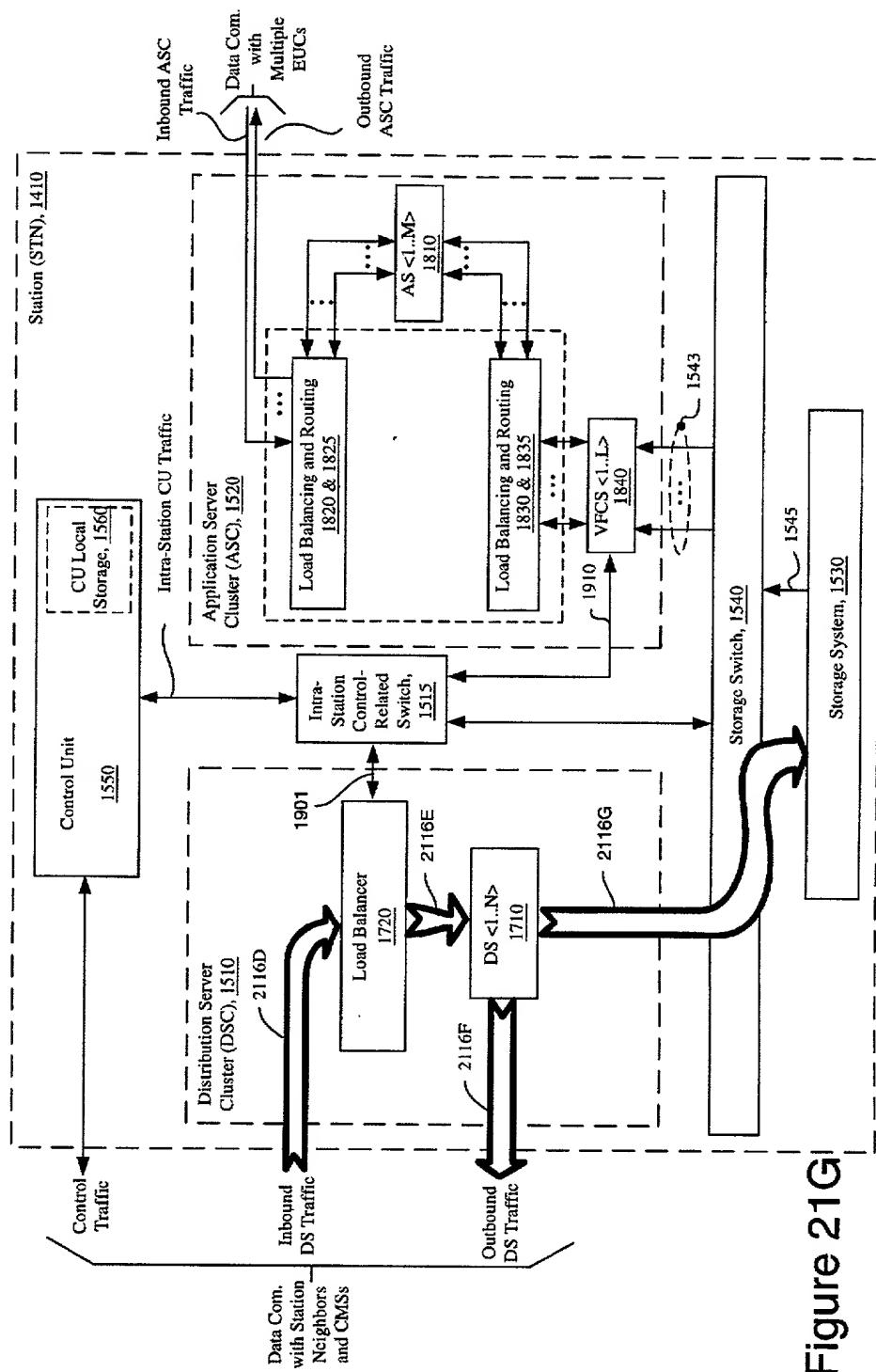
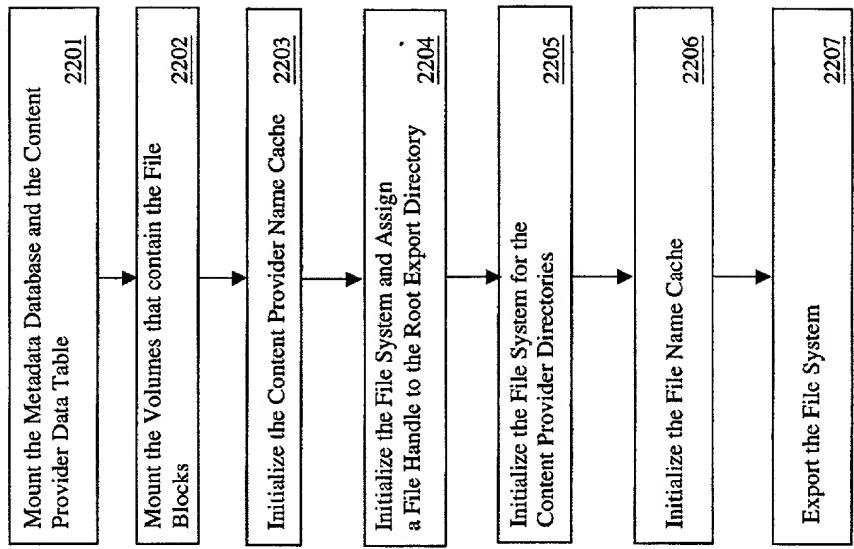


Figure 21G



**Figure 22**

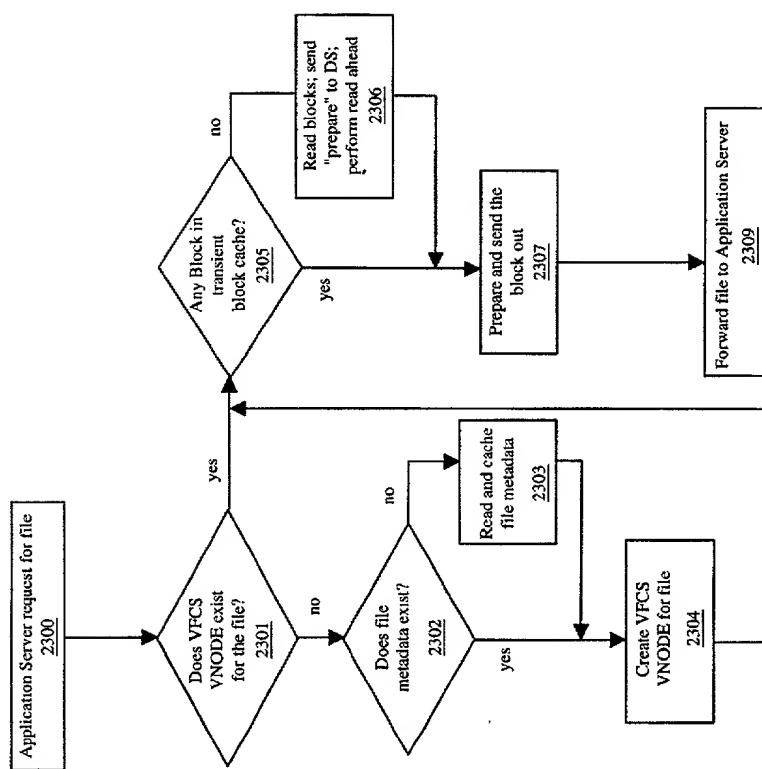


Figure 23

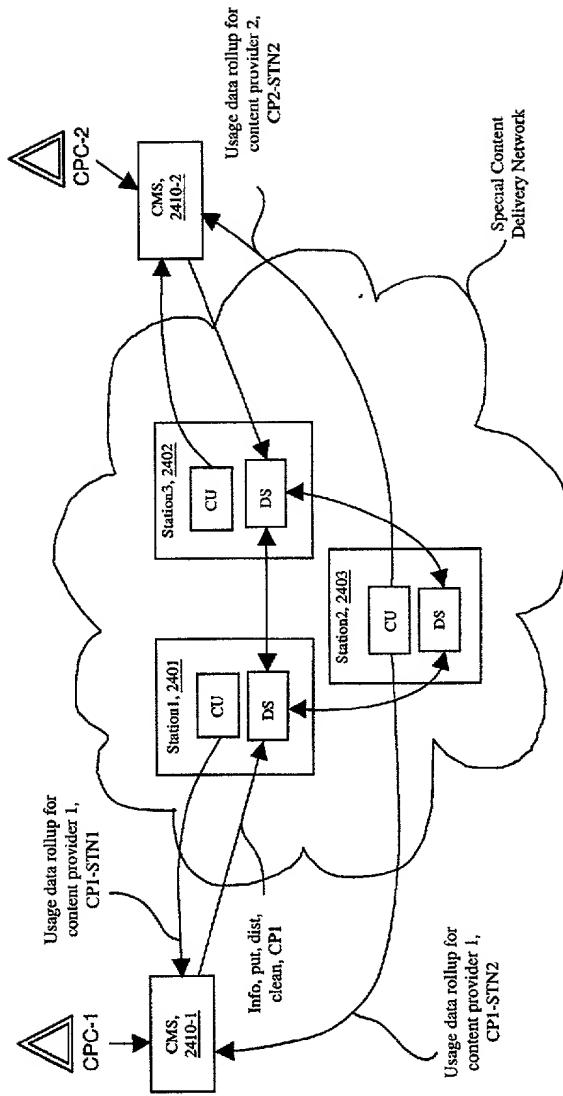


Figure 24

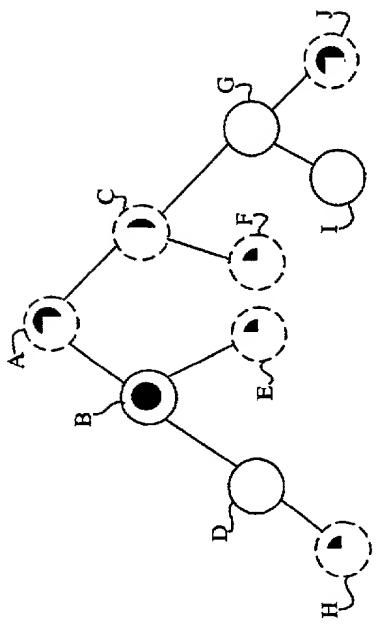


Figure 25